

Notic of References CitedApplication/Control No.
09/610,148Applicant(s)/Patent Under
Reexamination
KOBORI, ETSUYOSHIExaminer
Anh D. MaiArt Unit
2814

Page 1 of 1

U.S. PATENT DOCUMENTS

*		Document Number Country Code-Number-Kind Code	Date MM-YYYY	Name	Classification	
	A	US-5840606	11-1998	Lee	438	255
	B	US-				
	C	US-				
	D	US-				
	E	US-				
	F	US-				
	G	US-				
	H	US-				
	I	US-				
	J	US-				
	K	US-				
	L	US-				
	M	US-				

FOREIGN PATENT DOCUMENTS

*		Document Number Country Code-Number-Kind Code	Date MM-YYYY	Country	Name	Classification	
	N	JP-2001-144090	05-2001	Japan	Koji	H01L	21/3205
	O						
	P						
	Q						
	R						
	S						
	T						

NON-PATENT DOCUMENTS

*		Include as applicable: Author, Title Date, Publisher, Edition or Volume, Pertinent Pages)
	U	C. Verove et al., Dual Damascene Architectures Evaluation for the 0.18-micron Technology and Below. IEEE 2000, pp. 267-269.
	V	S. S. Lin et al., An Optimized Integration Scheme for 0.13-micron Technology Node Dual-Damascene Cu Interconnect. IEEE 2000, pp. 273-275.
	W	L. T. Koh et al., Low-Frequency Noise Measurement of Copper Damascene Interconnects. IEEE 2000, pp. 152-154.
	X	

*A copy of this reference is not being furnished with this Office action. (See MPEP § 707.05(a).)
Dates in MM-YYYY format are publication dates. Classifications may be US or foreign.